IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 13, 21-24, and 28-29 without prejudice or disclaimer in accordance with the following:

1.-14. (CANCELLED)

15. (PREVIOUSLY PRESENTED) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory;

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory; and

a selection unit which selects one of a first assignment state and a second assignment state for the cache memory in response to a control signal, wherein, when the first assignment state is selected by the selection unit, the second address space is assigned for the cache memory, and when the second assignment state is selected by the selection unit, a third address space that partially overlaps the first address space is assigned for the cache memory.

16. (CANCELLED)

17. (PREVIOUSLY PRESENTED) The computer according to claim 15, further comprising:

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to the computer through the bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received.

18.-19. (CANCELLED)

20. (PREVIOUSLY PRESENTED) The computer according to claim 15 further comprising a cache controller controlling the cache memory, the cache controller comprising:

a first unit performing a switching to allow the cache memory to act as the random access memory;

a second unit setting a range of the cache memory in which the cache memory is acting as the random access memory;

a third unit setting an address space of the random access memory; and

a fourth unit receiving a notification from the cache memory when an address space of the cache memory acting as the random access memory is accessed, and accessing an external storage device when an address outside the address space of the cache memory is accessed.

21.-24. (CANCELLED)

25. (PREVIOUSLY PRESENTED) A system which controls a cache memory that is connected to a main memory with a first address space of a memory map and capable of acting as a random access memory, comprising:

a determining unit which determines whether the cache memory is acting as the random access memory;

an assigning unit which assigns a second address space of the memory map, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory; and

a selection unit which selects one of a first assignment state and a second assignment state for the cache memory in response to a control signal, wherein, when the first assignment state is selected by the selection unit, the second address space is assigned for the cache memory, and when the second assignment state is selected by the selection unit, a third address space that partially overlaps the first address space is assigned for the cache memory.

26. (PREVIOUSLY PRESENTED) The system according to claim 25, further comprising:

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to a computer through the bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory

and an access request externally sent from an address outside the second address space of the cache memory is received.

27. (PREVIOUSLY PRESENTED) The system according to claim 25, further comprising a cache controller controlling the cache memory, the cache controller comprising:

a first unit performing a switching to allow the cache memory to act as the random access memory;

a second unit setting a range of the cache memory in which the cache memory is acting as the random access memory;

a third unit setting an address space of the random access memory; and

a fourth unit receiving a notification from the cache memory when an address space of the cache memory acting as the random access memory is accessed, and accessing an external storage device when an address outside the address space of the cache memory is accessed.

28.-29. (CANCELLED)